REMARKS/ARGUMENTS

Claims 1, 3-16 are pending in this application.

Applicants have received the Office Action dated September 5, 2006, which: 1) rejects claims 11, 12, and 16 under 35 U.S.C. § 102(b) as allegedly anticipated by Sytwu (U.S. Pat. No. 5,572,688) (hereinafter "*Sytwu*"); 2) rejects claims 1 and 3 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view of Clouser et al. (U.S. Pat. 5,884,053) (hereinafter "*Clouser*"); 3) rejects claim 4 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view *of Clouser* and Potter et al. (U.S. Pat. 6,533,587) (hereinafter "*Potter*"); 4) rejects claims 5 and 6 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view *of Clouser*, *Potter* and Intel Corporation (hereinafter "*Intel*"); 5) rejects claim 7 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view *of Clouser* and Shipe (U.S. Pat. 6,780,018) (hereinafter "*Shipe*"); 6) rejects claims 8-10 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view *of Clouser*, *Shipe* and Gehrke et al. (U.S. Pat. 6,310,992) (hereinafter "*Gehrke*"); 7) rejects claims 13-15 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Sytwu* in view of PCI-Express and *Clouser*.

With this Response, Applicants amend claims 1, 4, 7, 11. Therefore, claims 1, 3-16 remain pending. Based on these amendments, cancellations and the remarks that follow, Applicants submit that the pending claims are in condition for allowance and respectfully request reconsideration.

I. SECTION 102 REJECTIONS

Claims 11, 12, and 16 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by *Sytwu*.

Preliminarily, applicant notes that it is well settled that for a cited reference to qualify as prior art under 35 U.S.C. § 102, each element of the claimed invention must be disclosed within the reference. "It is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention." Hybritech, Inc., v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 231 U.S.P.Q. 81 (fed. Cir. 1986).

Applicant has very carefully studied the Examiner's comments and contentions set forth in the Official Action, but applicant respectfully traverses the Examiner's rejections for the reasons set forth below.

Claim 11 has been amended to recite:

> ...routing a second and different portion of the same bus to a first segment of a second slot. (emphasis added).

In *Sytwu*, the Office Action assumes and interprets two separate and distinct buses, namely a PCI bus (Figure 3, item 42) and an ISA bus (Figure 3, item 60) as being equivalent to the bus recited in claim 11. That construction of the claim is contrary to both the language of original claim 11, the language of ¶ [0012] which states in part "Bridge 12 also couples to PCI-Express slots 18A-B using the PCI-Express bus standard as disclosed in 'PCI-Express Base Specification 1.0a' ...", and also Figure 4 where data lanes belonging to the same bus and numbered "Lanes 16-23", "Lanes 8-15", and "Lanes 0-7" couple to slots 52A-C. As explained, the bus referred to in claim 11 is implemented as a bus using a single standard (PCI-Express), not a combination of standards (PCI/ISA) as interpreted by the Examiner. Moreover, *Sytwu* does not teach nor suggest a single bus implementation, but rather recites: "... the primary bus card 111 is connected to a PCI bus 42 (column 4, line 8) ...the secondary bus connector 114 is for connection to an ISA bus (column 4, line 11) ... the apparatus 110 of the invention is a single board that processes signals from two distinct buses (column 4, line12) ... the apparatus 110 of the invention provides a single device to process two sets of signals from two different buses (column 4, line 14) (emphasis added)." *Sytwu's* teaching directly contradict the language of claim 11 (as amended), which following proper antecedent basis and referring to the one and only bus mentioned at the beginning of the claim, recites: "routing a first portion of the bus..." (emphasis added), then "... routing a second and different portion of the same bus ..." (emphasis added). Therefore, constructing the claim as the Office Action does, as implementing a first bus (PCI) and a second distinct bus (ISA) is inaccurate.

Applicant has now amended the claim to make clear "the bus" referred to in the original claim means "the same bus". Claims 1, 4 and 7 have been similarly amended.

Furthermore, the Office Action suggests that item 111 in Figure 3 and Figure 4 in *Sytwu* is a jumper board. As defined, a jumper board typically allows for closing a circuit between two pins within the same slot. The jumper board described by Applicants in Figure 3B as item 44 and in ¶ [0027], closes multiple circuits among pairs of pins within the same slot 18A. A bus card, as described in *Sytwu*, is typically an expansion card used to physically extend a slot. *Sytwu* recites: "The primary bus card 111 includes a parallel port connector 64, a serial port connector 68, a floppy disk drive connector 72 (column 5, line 29), ...a hard disk drive controller 50 (column 5, line 35) ... having a set of signals traces 127 ... to process signals to and from the PCI bus 42 (column 5, lines 37-39)." Therefore, *Sytwu* does not teach, suggest or recite the functionality of the jumper board described by Applicants in ¶ [0027], but instead it teaches an expansion board 111 for a PCI bus 42 in Figure 3, Figure 4, and Figure 8. Thus, *Sytwu*'s teachings are directly contradictory to the language of claim 11. For at least these reasons, claim 11 is patentable over *Sytwu*.

Dependent claims 12 and 16 depend directly or ultimately on allowable claim 11 and are therefore allowable for at least this reason.

II. SECTION 103 REJECTIONS

Claims 1, 3-10, and 13-15 stand rejected under 35 U.S.C. § 103(a) as allegedly obvious over *Sytwu* in conjunction with at least one additional reference.

It is well known that for an obviousness-type rejection to stand, the cited document must disclose all aspects of the claimed invention; contain a suggestion to modify the cited document to arrive at the claimed invention; and there must be a reasonable chance of success.

The U.S. Court of Appeals for the Federal Circuit (C.A.F.C.) has set forth in Hodosh v. block Drug Co., 786 F.2d 1136, 1143 (Fed. Cir. 1986) what is

described as the "tenets of patent law that must be adhered to when applying § 103." Those tenets are:

> a) the claimed invention must be considered as a whole;
> b) the references must be considered as a whole and suggest the desirability and thus obviousness of making the combination;
> c) the references must be reviewed without the benefit of hindsight vision afforded by the claimed invention; and
> d) "ought to be tried" is not the standard with which obviousness is determined.

Additionally, in Harness International, Inc. v. Simplimatic Engineering Co., 2 USPQ2D 1826 (fed. Cir. 1987), the U.S. Court of Appeals for the Federal Circuit held that a dependent claim contains all the limitations of the claim it depends upon plus a further limitation, therefore a dependent claim is not obvious if the claim it depends upon is not obvious.

Applicants respectfully traverse this rejection because neither *Sytwu* nor any of the other references teach or suggest all of the claim elements. For example, independent claim 1, as amended, requires:

> ... a first slot configured to receive a device, wherein a first set of lanes of the bus is coupled to the first slot; a second slot configured to receive a device wherein a second and different set of lanes of the same bus is coupled to the second slot (emphasis added).

As suggested by the Office Action, in *Sytwu*, the bus coupled to the first slot (Figure 3, item 112) is a PCI 42 bus, whereas the bus coupled to the second slot (Figure 4, item 114) is an ISA bus 60. Thus, Sytwu's teachings are directly contradictory to the language of claim 1 (as amended), which requires that the bus coupled to the second slot be the same as the bus coupled to the first slot. Furthermore, ¶ [0012] and Figure 1 explain that bridge 12 couples to the slots 18A-B using the PCI-express bus not a combination of different bus standards such as PCI and ISA, as interpreted by the examiner. Moreover, the Office Action suggests that item 111 in Figure 3 and Figure 4 in *Sytwu* is a jumper

board. As defined, a jumper board typically allows for closing a circuit between two pins within the same slot. The jumper board described by Applicants in Figure 3B as item 44 and in ¶ [0027], closes multiple circuits among pairs of pins within the same slot 18A. A bus card, as described in *Sytwu*, is typically an expansion card used to physically extend a slot. *Sytwu* recites: "The primary bus card 111 includes a parallel port connector 64, a serial port connector 68, a floppy disk drive connector 72 (column 5, line 29), ...a hard disk drive controller 50 (column 5, line 35) ... having a set of signals traces 127 ... to process signals to and from the PCI bus 42 (column 5, lines 37-39)." Therefore, *Sytwu* does not teach, suggest or recite the functionality of the jumper board described by Applicants in ¶ [0027], but instead it teaches an expansion board 111 for a PCI bus 42 in Figure 3, Figure 4, and Figure 8. Thus, *Sytwu*'s teachings are directly contradictory to the language of claim 1. Therefore, *Sytwu* cannot render claim 1 obvious. Furthermore, the remainder of the cited art is similarly deficient in this regard and thus claim 1 and its dependent claims are patentable over the cited art for at least these reasons.

Claim 4 has been amended to recite:

> a first slot configured to receive a device, wherein a first set of lanes of the bus is coupled to the first slot;
> a second slot configured to receive a device, wherein a second and different set of lanes of the same bus is coupled to the second slot; at least one trace coupled to the first and second slots; and a jumper board;
> wherein the computer system is configured so that inserting the jumper board in the first slot couples the first set of lanes of the bus to the second slot, wherein the slots are implemented on a riser board (emphasis added).

As suggested by the Office Action, in *Sytwu*, the bus coupled to the first slot (Figure 3, item 112) is a PCI 42 bus, whereas the bus coupled to the second slot (Figure 4, item 114) is an ISA bus 60. Thus, Sytwu's teachings are directly

contradictory to the language of claim 4 (as amended), which requires that the bus coupled to the second slot be the same as the bus coupled to the first slot. Furthermore, ¶ [0012] and Figure 1 explain that bridge 12 couples to the slots 18A-B using the PCI-express bus not a combination of different bus standards, PCI and ISA, as interpreted by the examiner. Moreover, the Office Action suggests that item 111 in Figure 3 and Figure 4 in *Sytwu* is a jumper board. As defined, a jumper board typically allows for closing a circuit between two pins within the same slot. The jumper board described by Applicants in Figure 3B as item 44 and in ¶ [0027], closes multiple circuits among pairs of pins within the same slot 18A. A bus card, as described in *Sytwu*, is typically an expansion card used to physically extend a slot. *Sytwu* recites: "The primary bus card 111 includes a parallel port connector 64, a serial port connector 68, a floppy disk drive connector 72 (column 5, line 29), ...a hard disk drive controller 50 (column 5, line 35) ... having a set of signals traces 127 ... to process signals to and from the PCI bus 42 (column 5, lines 37-39)." Therefore, *Sytwu* does not teach, suggest or recite the functionality of the jumper board described by Applicants in ¶ [0027], but instead it teaches an expansion board 111 for a PCI bus 42 in Figure 3, Figure 4, and Figure 8. Thus, *Sytwu*'s teachings are directly contradictory to the language of claim 4. Therefore, *Sytwu* cannot render claim 4 obvious. Furthermore, the remainder of the cited art is similarly deficient in this regard and thus claim 4 and its dependent claims are patentable over the cited art for at least these reasons.

Claim 7 has been amended to recite:

> ... a first slot configured to receive a device, wherein a first set of lanes of the bus is coupled to the first slot; a second slot configured to receive a device, wherein a second and different set of lanes of the same bus is coupled to the second slot; at least one trace coupled to the first and second slots; wherein the computer system is configured so that inserting a jumper board in the first slot couples the first set of lanes of the bus

> to the second slot, wherein the first and second sets of lanes of the bus each form a serial bus; and wherein the slots are implemented together on a board other than the jumper board (emphasis added).

As suggested by the Office Action, in *Sytwu,* the bus coupled to the first slot (Figure 3, item 112) is a PCI 42 bus, whereas the bus coupled to the second slot (Figure 4, item 114) is an ISA bus 60. Thus, Sytwu's teachings are directly contradictory to the language of claim 7 (as amended), which requires that the bus coupled to the second slot be the same as the bus coupled to the first slot. Furthermore, ¶ [0012] and Figure 1 explain that bridge 12 couples to the slots 18A-B using the PCI-express bus not a combination of different bus standards, PCI and ISA, as interpreted by the examiner. Moreover, the Office Action suggests that item 111 in Figure 3 and Figure 4 in *Sytwu* is a jumper board. As defined, a jumper board typically allows for closing a circuit between two pins within the same slot. The jumper board described by Applicants in Figure 3B as item 44 and in ¶ [0027], closes multiple circuits among pairs of pins within the same slot 18A. A bus card, as described in *Sytwu*, is typically an expansion card used to physically extend a slot. *Sytwu* recites: "The primary bus card 111 includes a parallel port connector 64, a serial port connector 68, a floppy disk drive connector 72 (column 5, line 29), ...a hard disk drive controller 50 (column 5, line 35) ... having a set of signals traces 127 ... to process signals to and from the PCI bus 42 (column 5, lines 37-39)." Therefore, *Sytwu* does not teach, suggest or recite the functionality of the jumper board described by Applicants in ¶ [0027], but instead it teaches an expansion board 111 for a PCI bus 42 in Figure 3, Figure 4, and Figure 8. Thus, *Sytwu*'s teachings are directly contradictory to the language of claim 7. Therefore, *Sytwu* cannot render claim 7 obvious. Furthermore, the remainder of the cited art is similarly deficient in this regard and thus claim 7 and its dependent claims are patentable over the cited art for at least these reasons.

Because dependent claims 3, 5, 6, 8-10 and 13-15 depend directly or ultimately on allowable base claims, they are therefore allowable for this reason

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and by virtue of their further distinctive recitations over the cited references in any combination.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. However, if the Examiner wishes to resolve any other issues by way of a telephone conference, the Examiner is kindly invited to contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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